IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellants:	Cogdill et al.	Patent Application	
Application Number:	10/655,964	Group Art Unit:	2819
Filed:	September 4, 2003	Examiner:	Tran, J.

For: CIRCUIT AND SYSTEM FOR ADDRESSING MEMORY MODULES

APPEAL BRIEF

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I. Real Party in Interest

The assignee of the present invention is Hewlett-Packard Development Company, L.P.

II. Related Appeals and Interferences

There are no related appeals or interferences known to the Appellants.

III. Status of Claims

Claims 1-22 are rejected. This Appeal involves Claims 1-22.

IV. Status of Amendments

In compliance with 37 C.F.R. §1.116, an amendment subsequent to the Final Action has been filed, presenting rejected Claims in better form for consideration on appeal.

V. Summary of Claimed Subject Matter

Independent Claims 1, 8, and 14 of the present application pertain to embodiments associated with a circuit for a memory module address bus.

As recited in Claim 1, a "circuit for a memory module address bus" is disclosed. One embodiment is depicted at least in Figure 2. As described in the instant disclosure on at least page 6, lines 19-24 and page 8, lines 1-6, and Figure 2, one embodiment includes a transmission line 320 comprising a series dampening impedance 350 between a driver 305 and a branch point 315 of transmission line 320. The instant disclosure further includes at least on page 6, lines 19-24, page 7, lines 7-18, and Figure 2 a parallel termination impedance 360 having one end coupled to transmission line 320 between series dampening impedance 350 and branch point 315, wherein parallel termination impedance 360 is on a same side of all memory modules 340 as driver 305. Furthermore, the instant disclosure includes on at least page 6, lines 1-17, page 8, lines 1-6, and Figure 2 transmission line 320 having branches 320c and 320d from branch point 315, wherein ones of branches 320c are coupled to at least one memory module interface 330.

As recited in Claim 8, a "circuit for reducing skew when addressing a memory module" is disclosed. One embodiment is depicted at least in Figure 2. As described in the instant disclosure on at least page 6, lines 1-17, and Figure 2, one embodiment includes a plurality of memory modules 340. The instant disclosure further includes on at least page 6, lines 1-17, and Figure 2 an address line coupling memory modules 340. Furthermore, the instant disclosure includes on at least page 6, lines 19-24, page 7, lines 7-18, and Figure 2 a transmission line 320 having a series dampening impedance 350 and a parallel termination impedance 360 in a stub configuration (Figure 2), wherein parallel termination impedance

360 is on a same side of all memory modules 340 as a driver 305. Moreover, the instant disclosure further includes on at least page 6, lines 19-24, page 8, lines 1-6, and Figure 2 transmission line 320 having a first end coupled to driver 305 and a second end connected at a point 315 on address line to reduce skew when addressing a memory module 340.

As recited in Claim 14, a "system for addressing memory modules" is disclosed. One embodiment is depicted at least in Figure 2. As described in the instant disclosure on at least page 4, lines 11-14, and Figure 2, one embodiment includes a bus controller. The instant disclosure further includes at least on page 6, lines 19-24, page 8, lines 1-6, and Figure 2 a transmission line 320 comprising a series dampening impedance 350 between a driver 305 and a branch point 315 of transmission line 320. Furthermore, the instant disclosure includes on at least page 6, lines 19-24, page 7, lines 7-18, and Figure 2 a parallel termination impedance 360 having a first end coupled to transmission line 320 between series dampening impedance 350 and branch point 315 and a second end coupled to a termination voltage terminal 370, wherein parallel termination impedance 360 is on a same side of all memory modules 340 as a driver 305. Moreover, the instant disclosure further includes at least on page 6, lines 1-17, page 8, lines 1-6, and Figure 2 transmission line 320 having branches 320c, 320d from branch point 315, wherein ones of branches 320c are coupled to at least one memory module interface 330.

VI. Grounds of Rejection to Be Reviewed on Appeal

1. Claims 1-5, 7-19, and 21 are rejected under 35 U.S.C. §102(e) as being anticipated by Johnson et al. (U.S. Patent Application No. 6,715,014) (hereinafter, "Johnson").

2. Claims 6 and 20 are rejected under 35 U.S.C. §103(a), as being unpatentable over Johnson in view of Buuck et al. (U.S. Patent Application No. 5,583,449) (hereinafter, "Buuck").

3. Claim 22 is rejected under 35 U.S.C. §103(a) as being unpatentable over Johnson in view of Mizukami et al. (U.S. Patent Application No. 5,111,080) (hereinafter, "Mizukami").

VII. Argument

1. Whether Claims 1-5, 7-19, and 21 are patentable under 35 U.S.C. §102(e) over Johnson.

The Office Action Mailed on December 1, 2008 (hereinafter, "instant Office Action") states that Claims 1-5, 7-19, and 21 are rejected under 35 U.S.C. §102(e) as being anticipated by Johnson. The rejections and comments set forth in the instant Office Action have been carefully considered by the Appellants. Appellants respectfully submit that Claims 1-5, 7-19, and 21 are not anticipated by Johnson in view of at least the instant response.

Appellants respectfully point out that amended Claim 1 recites (Claims 8 and 14 include similar features):

> A circuit for a memory module address bus comprising:
> a transmission line comprising a series dampening impedance between a driver and a branch point of said transmission line; and
> a parallel termination impedance having one end coupled to said transmission line between said series dampening impedance and said branch point, wherein said parallel termination impedance is on a same side of all memory modules as said driver;
> said transmission line having branches from said branch point, wherein ones of said branches are coupled to at least one memory module interface.

Appellants respectfully note, "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference". MPEP §2131; *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 103 (Fed. Cir. 1987). … "The identical invention must be shown in as complete detail as is contained in the … claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). "The elements must be arranged as required by the claim…" *In re Bond*, 910 F.2d 831, 15 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The instant Office Action states that:

> Figure 3 of Johnson discloses a circuit for a memory module address bus comprising:… With respect to **claim 1**, a transmission line (314) comprising a dampening impedance (324) between a driver (312) and a branch point (node between 318 and 320, hereinafter "star node") of said transmission line (314); and
>
> a parallel termination impedance (326 – where 326 is parallel in reference to V_{TT} and star node) having one end coupled to said transmission line (314) between (see Figure 3b as shown above) said dampening impedance (324) and said branch point (star node), wherein said parallel termination impedance (326) is on a same side of any memory module as said driver (where Figure 3b shows 326 and driving source below the memory modules);
>
> said transmission line (314) having branches (316-322) from said branch point, wherein ones of said branches are coupled to at least one memory module interface (304).

(Emphasis in original; instant Office Action, page 5, second to last paragraph, through page 6, first paragraph.) Furthermore, the instant Office Action states, "The circuit as shown below (Figure 3b) is **equivalent** to the circuit shown in Figure 3 of Johnson" (emphasis added; instant Office Action, page 2, third paragraph).

Appellants respectfully submit that Johnson does not anticipate "a transmission line comprising a dampening impedance between a driver and a branch point of said transmission line; and a parallel termination impedance having one end coupled to said transmission line between said series dampening impedance and said branch point, wherein said parallel termination impedance is on a same side of all memory modules as said driver" (Emphasis added; Appellants' Claim 1.) Appellants understand Johnson, and more specifically Johnson's Figure 3, to disclose termination impedance that is not between the branch point and the dampening impedance.

As seen in Appellants' Figure 2 and described in Appellants' Claim 1, series dampening impedance 350 is between driver 305 and branch point 315 of transmission line 320b. Parallel termination impedance 360 has one end coupled to transmission line 320b between series dampening impedance 350 and branch point 315, and parallel termination impedance 360 is on the same side of all memory modules 330 as driver 305. However, Johnson's Figure 3 shows a parallel termination impedance 326 having one end coupled to a branch point, while the other end is coupled to the termination voltage.

Therefore, Appellants respectfully submit that Johnson does not anticipate "a parallel termination impedance having one end coupled to said transmission line between said series dampening impedance and said branch point, wherein said parallel termination impedance is on the same side of all memory modules as said driver" (emphasis added) as is recited in Appellants' Claim 1.

Therefore, Appellants respectfully submit that Johnson does not anticipate the features as are set forth in independent Claim 1, and as such, Claim 1 traverses the rejection under 35 U.S.C. §102(e) and is condition for allowance. Accordingly, Appellants also respectfully submit that Johnson does not anticipate Claims 8 and 14 for reasons stated herein regarding Claim 1. Furthermore, Appellants respectfully submit that Claims 2-5 and 7 depending on Claim 1, Claims 9-13 depending on Claim 8, and Claims 15-19 and 21 depending on Claim 14 overcome the rejection under 35 U.S.C. §102(e) as being dependent on an allowable base Claim.

2. Whether Claims 6 and 20 are patentable under 35 U.S.C. §103(a) over Johnson in view of Buuck.

The instant Office Action rejected Claims 6 and 20 under 35 U.S.C. §103(a) as being unpatentable over Johnson in view of Buuck. The rejections and comments set forth in the instant Office Action have been carefully considered by the Appellants. Appellants respectfully submit that Claims 6 and 20 are patentable over Johnson in view of Buuck for at least the following rationale.

Appellants respectfully submit that the combination of Johnson and Buuck does not satisfy the requirements of a *prima facie* case of obviousness because the features of Claims 6 and 20 as a whole would not have been obvious over the combination of Johnson and Buuck.

"As reiterated by the Supreme Court in *KSR*, the framework for the objective analysis for determining obviousness under 35 U.S.C. 103 is stated in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966). Obviousness is a question of law based on underlying factual inquiries" including "[a]scertaining the differences between the claimed invention and the prior art" (MPEP 2141(II)). "In determining the differences between the prior art and the claims, the question under 35 U.S.C. 103 is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious" (emphasis in original; MPEP 2141.02(I)).

Appellants respectfully note that "[t]he prior art reference (or references when combined) need not teach or suggest all the claim limitations. However, Office personnel must explain why the difference(s) between the prior art and the claimed invention would have been obvious to one of ordinary skill in the art" (emphasis added; MPEP 2141[III]).

As presented above, Appellants respectfully submit that Johnson does not teach "a parallel termination impedance having one end coupled to said transmission line between said series dampening impedance and said branch point, wherein said parallel termination impedance is on a same side of all memory modules as said driver" (emphasis added) as is recited in Appellants' Claim 1. Appellants' specification describes at least one advantage for the positioning of its parallel termination impedance. For example:

> Referring briefly to Figure 1, the purpose of the pull-up parallel termination resistor 130 is to terminate the signal at the end of the transmission line 115. As such, it is not considered intuitive to place a parallel termination resistor on the same side of the memory modules as the driver. Referring now to Figure 2, the termination impedance 360 is placed on the same side of the memory modules 340 as the driver 305. As positioned, the combination of the series dampening impedance 350 and the parallel termination impedance 360 prevents, or at least reduces, reflections from the memory modules 340 from travelling back to the driver 305 in the region of the transmission line 320a between the parallel termination resistor 360 and the driver 305. There may be some reflections in the region of the transmission line 320b between the parallel termination resistor 360 and the branch point 315, as well as on the branches of the transmission line 320c and 320d.
>
> However, embodiments of the present invention are configured such that reflections between the parallel termination resistor 360 and the memory modules 340 do not cause significant signal integrity problems. For example, the memory modules 340 are located very close to each other relative to the size of the wavelength of a typical signal.

(Appellants' specification, second and third paragraph.)

In contrast, Johnson's termination impedance is not in between the dampening impedance (324) and the branch point. (See Johnson's Figure 3.) Furthermore, Appellants respectfully submit that the combination of Johnson and Buuck fails to suggest the features of Appellants' Claim 1 as a whole.

Appellants understand Buuck to teach the "cancellation of line reflections in a clock distribution network" (Buuck, Title.) Specifically, Buuck does not teach, describe, or suggest "a parallel termination impedance having one end coupled to said transmission line between said series dampening impedance and said branch point, wherein said parallel termination impedance is on a same side of all memory modules as said driver" (emphasis added) as is recited in Appellants' Claim 1.

Additionally, Appellants respectfully submit that the instant Office Action does not explain why the differences between Johnson, Buuck, and Appellants' claimed features would have been obvious to one or ordinary skill in the art.

Thus, in view of the combination of Johnson and Buuck not satisfying the requirements of a *prima facie* case of obviousness, Appellants respectfully assert that Claim 1 is patentable. Furthermore, Appellants respectfully submit that Claim 14 is also patentable for reasons stated herein regarding Claim 1. Moreover, Appellants respectfully submit that Claim 6 depending on Claim 1, and Claim 20 depending on Claim 14 are patentable as being dependent upon an allowable base Claim.

3. Whether Claim 22 is patentable under 35 U.S.C. §103(a) over Johnson in view of Buuck, in further view of Mizukami.

The instant Office Action rejected Claim 22 under 35 U.S.C. §103(a) as being unpatentable over Johnson in view of Mizukami. The rejections and comments set forth in the instant Office Action have been carefully considered by the Appellants. Appellants

respectfully submit that Claim 22 is patentable over Johnson in view of Mizukami for at least the following rationale.

Appellants respectfully submit that the combination of Johnson and Mizukami does not satisfy the requirements of a *prima facie* case of obviousness because the features of Claim 22 as a whole would not have been obvious over the combination of Johnson and Mizukami.

As presented above, Appellants respectfully submit that Johnson does not teach or suggest "a parallel termination impedance having one end coupled to said transmission line between said series dampening impedance and said branch point, wherein said parallel termination impedance is on a same side of all memory modules as said driver" (emphasis added) as is recited in Appellants' Claim 1. Furthermore, Appellants respectfully submit that the combination of Johnson and Mizukami fails to suggest the features of Appellants' Claim 1 as a whole.

Appellants understand Mizukami to teach a "complementary signal transmission circuit with impedance matching circuitry" (Mizukami, Title.) Specifically, Mizukami does not teach, describe, or suggest "a parallel termination impedance having one end coupled to said transmission line between said series dampening impedance and said branch point, wherein said parallel termination impedance is on a same side of all memory module as said driver" (emphasis added) as is recited in Appellants' Claim 1.

Additionally, Appellants respectfully submit that the instant Office Action does not explain why the differences between Johnson, Mizukami, and Appellants' claimed features would have been obvious to one or ordinary skill in the art.

Thus, in view of the combination of Johnson and Mizukami not satisfying the requirements of a *prima facie* case of obviousness, Appellants respectfully assert that Claim 1 is patentable. Furthermore, Appellants respectfully submit that Claim 14 is also patentable for reasons stated herein regarding Claim 1. Moreover, Appellants respectfully submit that Claim 22 depending on Claim 14 is patentable as being dependent upon an allowable base Claim.

CONCLUSION

Appellants believe that pending Claims 1-22 are directed toward patentable subject matter. As such, Appellants respectfully request that the rejections of Claims 1-22 be reversed.

The Appellants wish to encourage the Examiner or a member of the Board of Patent Appeals to telephone the Appellants' undersigned representative if it is felt that a telephone conference could expedite prosecution

Respectfully submitted,
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Dated: 03/30/2009

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VIII. Appendix - Clean Copy of Claims on Appeal

We claim:

1. A circuit for a memory module address bus comprising:

a transmission line comprising a series dampening impedance between a driver and a branch point of said transmission line; and

a parallel termination impedance having one end coupled to said transmission line between said series dampening impedance and said branch point, wherein said parallel termination impedance is on a same side of all memory modules as said driver;

said transmission line having branches from said branch point, wherein ones of said branches are coupled to at least one memory module interface.

2. The circuit of Claim 1, wherein said transmission line is uni-directional.

3. The circuit of Claim 1, wherein said ones of said branches are coupled to two memory module interfaces.

4. The circuit of Claim 1, wherein said ones of said branches are coupled to three memory module interfaces.

5. The circuit of Claim 1, wherein said ones of said branches are coupled to four memory module interfaces.

6. The circuit of Claim 1, wherein the distance from said branch point to said one end of said parallel termination impedance is greater than the length of said branches.

7. The circuit of Claim 1, wherein said one end of said parallel termination impedance is connected to said series dampening impedance.

8. A circuit for reducing skew when addressing a memory module comprising:

a plurality of memory modules;

an address line coupling said memory modules;

a transmission line having a series dampening impedance and a parallel termination impedance in a stub configuration, wherein said parallel termination impedance is on a same side of all memory modules as a driver; and

said transmission line having a first end coupled to said driver and a second end connected at a point on said address line to reduce skew when addressing a memory module.

9. The circuit of Claim 8, wherein said second end of said transmission line is connected at substantially the midpoint of said address line.

10. The circuit of Claim 8, wherein said transmission line is uni-directional.

11. The circuit of Claim 8, wherein said parallel termination impedance is connected to said series dampening impedance.

12. The circuit of Claim 8, wherein said plurality of memory modules is an odd number and wherein said second end of said transmission line is connected to said address line at the middle memory module.

13. The circuit of Claim 8, wherein said plurality of memory modules is an even number and wherein said second end of said transmission line is connected to said address line at a point substantially midway between two memory modules closest to the mid-point of said address line.

14. A system for addressing memory modules comprising:

a bus controller;

a transmission line comprising a series dampening impedance between a driver and a branch point of said transmission line; and

a parallel termination impedance having a first end coupled to said transmission line between said series dampening impedance and said branch point and a second end coupled to a termination voltage terminal, wherein said parallel termination impedance is on a same side of all memory modules as a driver;

said transmission line having branches from said branch point, wherein ones of said branches are coupled to at least one memory module interface.

15. The system of Claim 14, wherein two branches of said branches from said branch point have substantially the same length.

16. The system of Claim 14, wherein said transmission line is uni-directional.

17. The circuit of Claim 14, wherein said ones of said branches are coupled to two memory module interfaces.

18. The system of Claim 14, wherein said ones of said branches are coupled to three memory module interfaces.

19. The system of Claim 14, wherein said ones of said branches are coupled to four memory module interfaces.

20. The system of Claim 14, wherein the distance from said branch point to said first end of said parallel termination impedance is greater than the length of said branches.

21. The system of Claim 14, wherein said first end of said parallel termination impedance is connected to said series dampening impedance.

22. The system of Claim 14, wherein said parallel termination impedance and said series dampening resistance are mounted on opposite sides of a printed circuit board.

IX. Evidence Appendix

No evidence is herein appended.

X. Related Proceedings Appendix

No related proceedings.